## Remarks

Claims 1-11 were pending in the above-identified application when last examined. Claim 4-6 and 10-11 are canceled. Claim 1-3 and 7-9 are presented for reconsideration and allowance.

The Examiner rejected claims 1- 2 and 7-9 under 35 U.S.C. § 102(b) as being anticipated by Doh et al. (EP $_1$ 187 373 A2, hereinafter "Doh").

With regard to claim 1, Doh discloses, in Fig. 1, two separate and independent gain stages. The first gain stage, 12, is a low noise amplifier and the second gain stage, 13, is a limiting amplifier. An embodiment of this invention teaches the use of a clock data recovery block ("CDR") instead of using a second gain stage as shown in Fig. 1 of Doh. Because claim 1 does not require more than one gain stage, claim 1 is believed to be allowable.

The Examiner, in his response (Final Office Action, page 6), notes that the standing rejections apply to amplifiers 12 and 13 of Doh et al. together as a single gain stage. Applicants respectfully disagree. Each of the amplifiers, 12 and 13, create voltage gain and as a result they each may be considered gain stages. One advantage of the current invention is that it only uses one gain stage. By making use of only one gain stage, the power consumed by an optical receiver is reduced and the area required to implement an optical receiver is reduced.

For at least the above reason, Applicants request reconsideration and withdrawal of the rejection of Claim 1 under 35 U.S.C. § 102(b).

Furthermore, dependent claims 2 and 3 further define patentably distinct

independent claim 1. Therefore, claims 2 and 3 are also believed to be allowable. For at least this reason, Applicants request reconsideration and withdrawal of the rejection of claims 2 and 3.

Examiner rejected Claims 4-6 and 10-11 under 35 U.S.C. 103(a) as being unpatentable over Doh and further in view of Swenson et al. (U.S. Patent Application Publication No. US 2005/0191059 A1, hereinafter, "Swenson"). Claims 4-6 and 10-11 are canceled rendering their rejection moot.

With regard to claim 7, Doh discloses, in Fig. 1, two separate and independent gain stages. The first gain stage, 12, is a low noise amplifier and the second gain stage, 13, is a limiting amplifier. An embodiment of this invention teaches the use of a clock data recovery block ("CDR") instead of using a second gain stage as shown in Fig. 1 of Doh. Because claim 7 does not require more than one gain stage, claim 7 is believed to be allowable.

The Examiner, in his response (Final Office Action, page 6), notes that the standing rejections apply to amplifiers 12 and 13 of Doh et al. together as a single gain stage. Applicants respectfully disagree. Each of the amplifiers, 12 and 13, create voltage gain and as a result they each may be considered gain stages. One advantage of the current invention is that it only uses one gain stage. By making use of only one gain stage, the power consumed by an optical receiver is reduced and the area required to implement an optical receiver is reduced.

For at least the above reason, Applicants request reconsideration and withdrawal of the rejection of Claim 7 under 35 U.S.C. § 102(b).

Furthermore, dependent claims 8 and 9 further define patentably distinct independent claim 7. Therefore, Claims 8 and 9 are also believed to be allowable. For at least this reason, Applicants request reconsideration and withdrawal of the rejection of claims 8 and 9.

## Conclusion

Applicants respectfully submit that Applicants' pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby requested.

Respectfully submitted,

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/John Pessetto/

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